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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION--ETC(U)
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LEVEL II

INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION — PHASE III

SUMMARY REPORT NO. 3

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY · ST. LOUIS

MCDONNELL DOUGLAS CORPORATION

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INTEGRATED CIRCUIT ELECTROMAGNETIC SUSCEPTIBILITY INVESTIGATION PHASE III

5 JANUARY 1979

REPORT MDC E1999

SUMMARY REPORT NO. 3

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SUBMITTED TO THE CONTRACTING OFFICER, U.S. NAVAL SURFACE WEAPONS CENTER – DAHLGREN LABORATORY, DAHLGREN, VIRGINIA, 22448
UNDER CONTRACT NO. N60921-76-C-A030

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PREFACE

The work reported in this document was performed under Contract No. N60921-76-C-A030 for the U.S. Naval Surface Weapons Center, Dahlgren Laboratory, Dahlgren, Virginia 22448. The McDonnell Douglas Astronautics Company personnel involved were:

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1. INTRODUCTION AND SUMMARY

The U. S. Naval Surface Weapons Center — Dahlgren Laboratory (NSWC/Dahlgren) is tasked to provide electromagnetic compatibility (EMC) guidance for designers of electronic systems that must operate in high power electromagnetic environments. The program involves the development of technology in the following areas:

a. the susceptibility of discrete semiconductor components to microwave signals,
b. the susceptibility of integrated circuits (IC's) to microwave signals,
c. the electromagnetic environment,
d. electromagnetic pickup (coupling) and shielding.

All of the technology developed under this program will be included in MIL-HDBK-253 (Appendix) which will be published by the U.S. Navy.

The McDonnell Douglas Astronautics Company (MDAC), under contract to NSWC/Dahlgren, has developed the technology on the susceptibility of integrated circuits to microwave signals. This report summarizes the work performed in the last of three increments which together form the third and last phase of this program.

The primary output of the Integrated Circuit Electromagnetic Susceptibility (ICES) Investigation has been the ICES Handbook[1], which was published 1 August 1978. The handbook summarizes the susceptibilities of integrated circuits in a simplified format for use by electronics designers and others concerned with electromagnetic compatibility of electronic systems. Approximately 500 copies of the handbook were distributed to persons who have shown interest in the IC susceptibility program, and another 200 copies were mailed directly to NSWC/Dahlgren.

Several modifications were incorporated in the IC Handbook that were not included in earlier draft versions. The handbook contains additional measured susceptibility data, with significant expansions in the data for line drivers and receivers, comparators and voltage regulators. The modeling sections of the handbook were greatly expanded, and include examples of modeling interference in TTL NAND gates and bipolar operational amplifiers. A brief chapter was added which discussed coupling and shielding phenomena to make the handbook more nearly a self-contained reference for EMC applications. Chapter 2 of this report describes the handbook revisions in greater detail.

Chapter 3 describes the IC susceptibility measurements that were made during this increment. Op amps, line drivers and receivers, voltage regulators, and comparators were tested. Susceptibility data from the tests were included in the handbook susceptibility section.

Much modeling activity, ranging from models of rectification in PN junctions to interference models of complete integrated circuits, occurred during this increment. This work is described in Chapter 4. Rectification in PN junctions is described with two models: a Fourier technique, and a much simpler circuit model. Detailed accounts of modeling interference in integrated circuit NAND gates and op amps is also given. An analysis of signal quality in data transmission systems involving line drivers and receivers is described, which shows that data transmission rates may have to be reduced in order to ensure quality data transmission in intense electromagnetic environments.

Two electromagnetic susceptibility seminars were held during this increment, sponsored jointly by MDAC and NSWC/Dahlgren. Chapter 5 briefly describes these seminars.

2. IC SUSCEPTIBILITY HANDBOOK REVISION

In August 1978, the final version of the Integrated Circuit Electromagnetic Susceptibility Handbook[1] was published and distributed. This report summarized all of the susceptibility information which had been obtained during this contract in a handbook format for ready use by EMC engineers and system designers. Comments received from earlier versions of this handbook were incorporated wherever possible.

The latest Handbook version used a revised format over earlier versions. Separate chapters were devoted to component susceptibility data, modeling information, coupling and shielding information, and information on interference reduction techniques. The system hardening task flow chart, shown in Figure 1, was modified to reflect the Handbook reorganization. The new flow chart shows clearly where different sections of the Handbook are best used in the system hardening task.

A chapter on coupling and shielding considerations was added as an aid to users of the Handbook, since pickup levels and shielding must be measured or estimated in order to evaluate system susceptibility to external RF fields. Enough information is presented to allow the

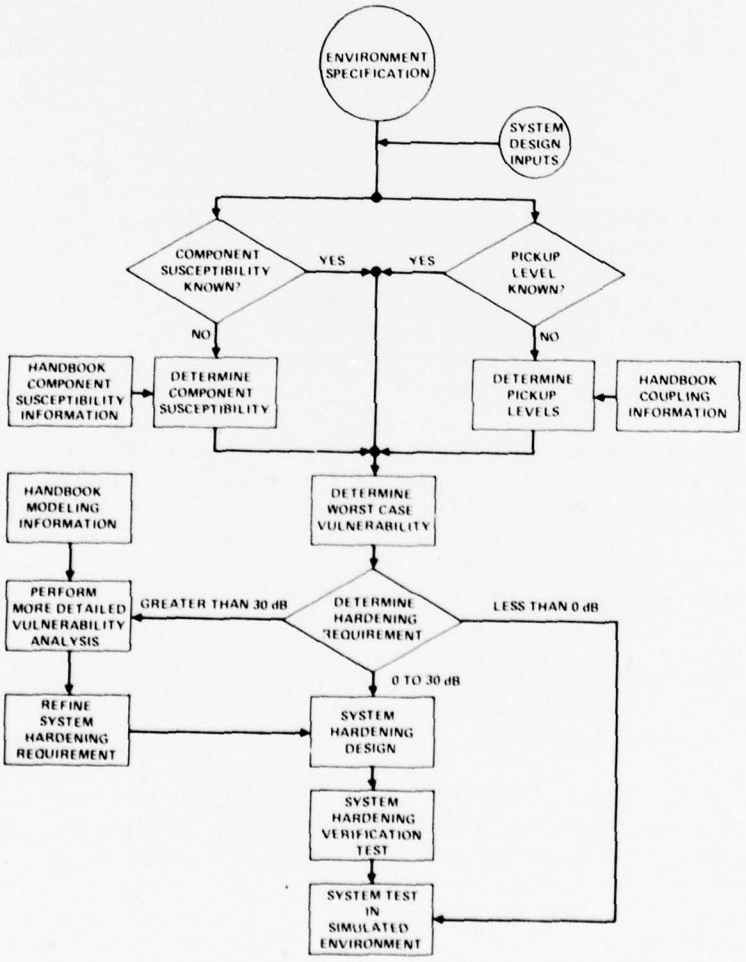


Figure 1. System Hardening Task Flow

system designer to make an initial estimate of pickup levels in his system using the relationship $A_e = 0.13 \lambda^2$ for the effective aperture of unshielded wires. The statistical aspects of both coupling and shielding are also stressed to describe the variations of pickup with wire position and aspect angle. Shielding effectiveness is treated as a shift in the probability density function of the pickup level of a wire with and without shielding.

The final version of the handbook contains much susceptibility information not contained in earlier versions. A short discussion of package effects was added which explicitly states that no package type shows any significant advantage in susceptibility reduction over other types. New susceptibility data was presented for line drivers and receivers, voltage regulators, and comparators. In addition, theoretical information on signal quality vs. data rate for digital data transmission systems illustrates that reduced data rates may be necessary to ensure quality signals when interference is present. A slight revision in the worst case op amp susceptibility curve was made to include new susceptibility data at 9.1 GHz (which lowered the worst case levels at this frequency by about 4 dB). From the modeling efforts, theoretically predicted worst case levels were developed for TTL devices, and these levels were added to the TTL worst case susceptibility graph. These changes are described in more detail in later sections of this report.

A considerable amount of new modeling information was added to the final version of the Handbook. While the diode rectification model and modified Ebers-Moll transistor model remained unchanged, the theoretical ranges of the model parameters were generalized. Also added was a worst case study of interference in a 7400 NAND gate. The study used previously developed rectification models and the program SPICE to calculate the minimum RF power levels at which interference is possible. The program was also used to compare the susceptibilities of the standard TTL family to the low power (74L00) and high speed (74H00) TTL families. A modeling simulation of interference in a 741 op amp, was performed using ISPICE, a commercially available timesharing version of SPICE, and macromodeling techniques to analyze interference at the input terminals of an op amp, and compare these results to those obtained when a simple offset model is used.

The Handbook chapter on interference reduction techniques was expanded. The effectiveness of component screening to choose less susceptible devices was discussed, with the ultimate conclusion that component screening can be used, but should be used only after more conventional interference reduction schemes are attempted (shielding, filtering, etc.). The Handbook contains an expanded section on less susceptible circuit designs, which describes many of the options available to the circuit designer to reduce the susceptibility of electronic circuits.

3. IC SUSCEPTIBILITY MEASUREMENTS

The purpose of the integrated circuit susceptibility testing was to verify, and refine wherever necessary, previously published minimum susceptibility levels. The results of tests of op amps, line drivers and receivers, voltage regulators, and comparators are included in this chapter. Where necessary, special test techniques were used to assess the ability of the integrated circuit to operate with the applied RF stimulus. Only a modicum of susceptibility information was available previously for some devices, and the additional susceptibility information was included in the Integrated Circuit Electromagnetic Susceptibility Handbook.

3.1 Interference in Op Amps — Additional laboratory testing of op amp susceptibilities was performed during this increment. Tests at 0.22, 3.0, and 5.6 GHz verified the minimum susceptibility levels previously published. At 9.1 GHz, however, the minimum susceptibility level was reduced by 4 dB. Figure 2 shows the final estimate of worst case susceptibility values for op amps.

3.2 Interference in Line Drivers and Receivers — Line drivers and receivers are used to transmit digital data over long system interconnect cables in aerospace systems. Line drivers and receivers were tested to determine their susceptibilities to RF energy. The drivers and receivers were tested independently in order to single out those characteristics of each which, when altered by RF, would adversely affect system performance (such as a decrease in system noise margin).

All of the line drivers tested were differential line drivers, i.e., each drives two complementary output lines. Drivers with open collector outputs were tested as well as types containing active pullups. Susceptibility criteria were established based on manufacturers' specifications for the output voltage at each output terminal. Each output terminal was considered separately, and the device was considered susceptible if either output crossed the appropriate interference threshold. Figure 3 illustrates the worst case susceptibility values measured for line drivers.

Receiver susceptibilities were defined in terms of changes in the input voltage threshold which determines the receiver switchpoint (where the input voltage is measured differentially between the two input terminals). Input voltage threshold changes were used as the susceptibility criteria during the testing. Changes in the input voltage threshold represent decreased system noise margins, and possible malfunction of the data link. Figure 4 shows the minimum susceptibility levels for line receivers.

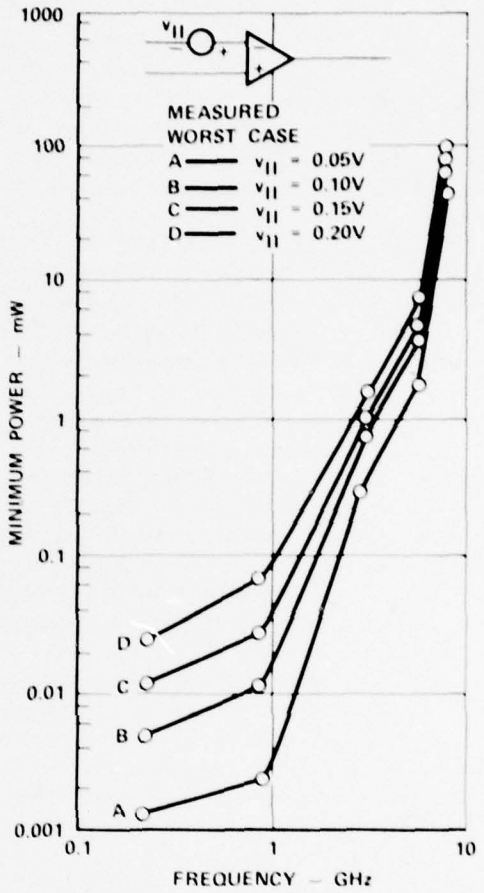


Figure 2. Worst Case Susceptibility Values for Op Amps

Line receivers are generally used in conjunction with line drivers. Comparison of Figures 3 and 4 shows receivers approximately 7 dB more susceptible than line drivers. If a line driver and receiver are considered as a system, the susceptibility of the pair is adequately described by the susceptibiity of the receiver only, as shown in Figure 4. In the ICES Handbook, this figure was used to define the susceptibility levels of line driver and receiver pairs. The receiver input voltage threshold was retained as the susceptibility criterion.

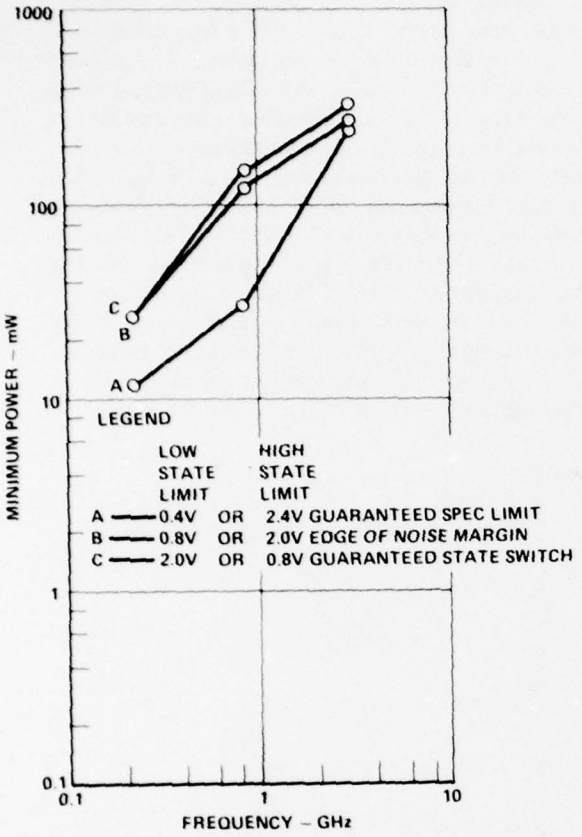


Figure 3. Worst Case Susceptibility Values for Line Drivers

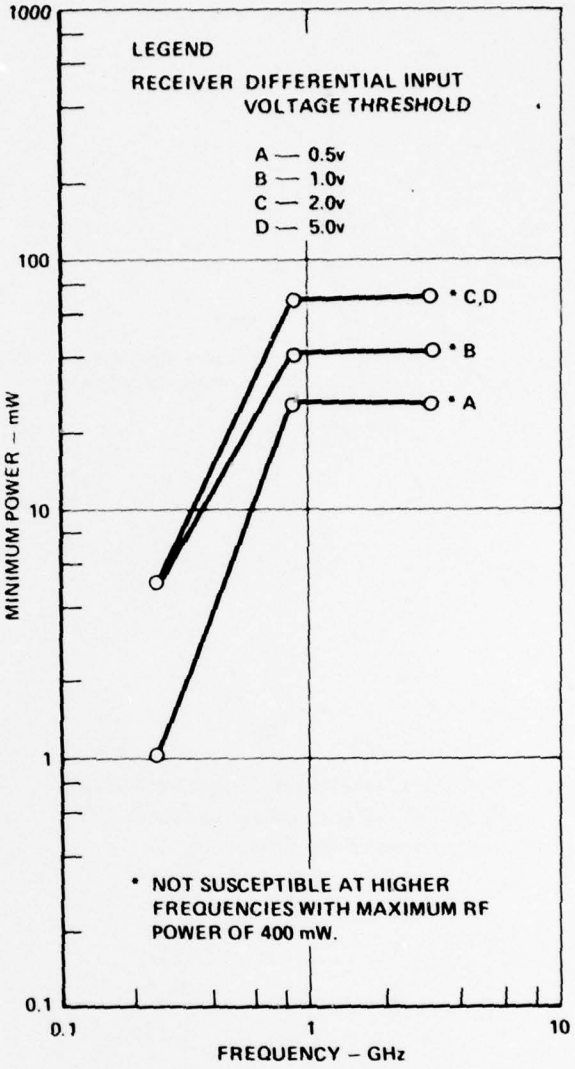


Figure 4. Worst Case Susceptibility Values for Line Receivers

3.3 Interference in Voltage Regulators — Integrated circuit voltage regulators were tested during this increment to determine their susceptibilities to RF energy and to supplement previously published susceptibility data. Voltage regulators may be separated into two distinct categories: 3-pin and multi-pin devices. The 3-pin voltage regulators have (as their name implies) only three pins, and feature fixed output voltages and convenience of use because they generally require no external elements. The multi-pin regulators have more than 3 pins (4, 8 or 10 pin devices are common) and are more versatile than the 3-pin regulators. By appropriate connections of external elements, variable output voltages or different regulator configurations may be obtained with the multi-pin regulators.

Three-pin voltage regulators having a nominal output voltage of 5 volts, and 8-pin regulators were tested. The 8-pin regulators were tested in a configuration with a nominal output voltage of 12 volts. The susceptibility criterion was an output voltage deviation of 0.25 volts from nominal. The 3-pin regulators were approximately 12 dB less susceptible than the multi-pin regulators. Figure 5 shows the susceptibilities of the 3-pin and multi-pin regulators.

Figure 6 illustrates why 3-pin regulators are less susceptible than multi-pin regulators. A basic regulator circuit is shown, which contains a resistive divider, an op amp, and a series pass element. In multi-pin regulators the resistive divider is external to the chip, and the amplifier input (the most susceptible terminal) is available as an integrated circuit terminal. (Operational amplifiers are known to be quite susceptible to RF conducted into their inputs[1].) In the 3-pin regulators, the

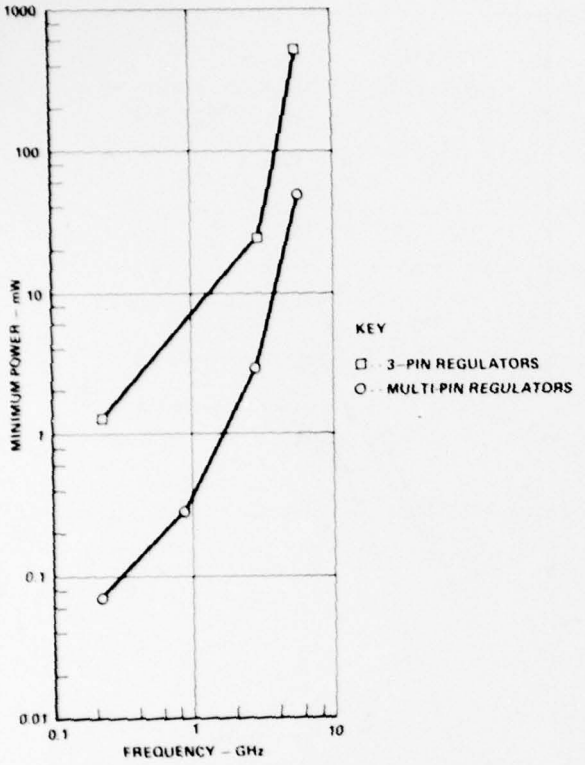


Figure 5. Worst Case Susceptibility Values for Voltage Regulators. Output Voltage Change of 0.25 Volt is Susceptibility Criterion.

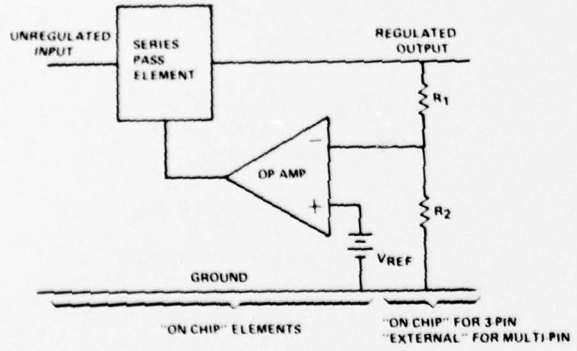


Figure 6. Basic Series Regulator Circuit

resistive divider is contained on the regulator chip, and the amplifier terminals are not accessible, so these devices are less susceptible.

3.4 Interference in Comparators — Measurements were made of the RF susceptibility of voltage comparators. Susceptibility was defined in terms of changes in the comparator switchpoint. An offset in the comparator switchpoint has an adverse effect on the comparator's accuracy when used to detect voltage levels in circuits.

Figure 7 illustrates the minimum susceptibility values observed for comparators. The devices were most susceptible to RF conducted into the input terminals. This is expected, since comparators contain a differential pair input stage similar to that contained in op amps. Comparison of Figure 7 with Figure 2 shows the similarity in susceptibility levels of the two device types.

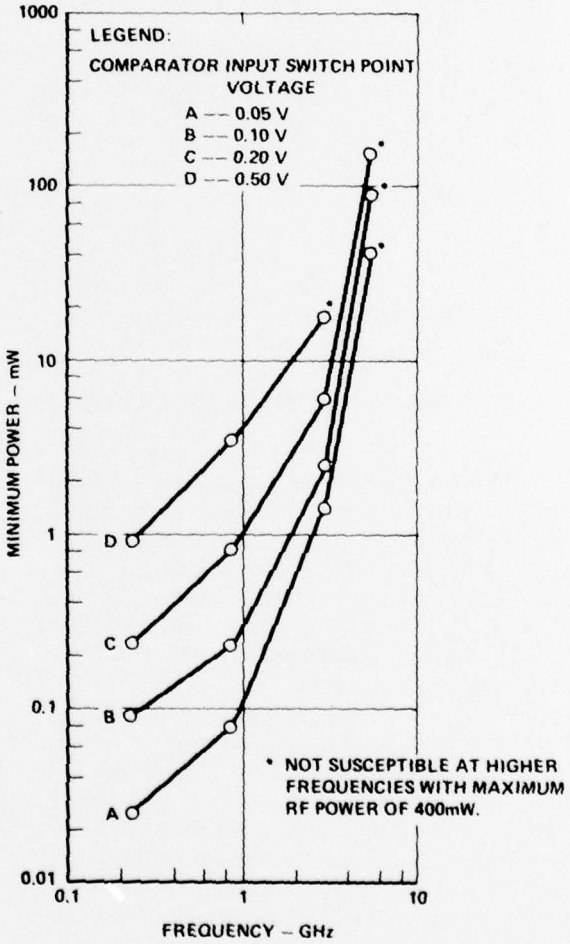


Figure 7. Worst Case Susceptibility Values for Comparators

4. INTERFERENCE EFFECTS

During this increment, the interference effects in integrated circuits were modeled. This chapter summarizes the work that was performed, including investigations into the basic interference mechanism: rectification in PN junctions.

4.1 Diode Rectification Measurements — Rectification in PN junctions has been determined to be the principal source of interference in modern electronic circuits. However, because of the nonlinear nature of semiconductor junctions, an analytical approach to studying rectification becomes quite involved, except for the small signal case where simplifying assumptions can be made.

The current rectification efficiency of several representative diodes was measured versus bias voltage, RF power level, and frequency. The current rectification efficiency, η (eta), is defined as

$$\eta = (i_{RF} - i_{no\ RF})/P_{RF}, \quad (1)$$

where i_{RF} is the dc component of diode current when the RF signal is applied,
$i_{no\ RF}$ is the diode current when no RF signal is present, and
P_{RF} is the RF power level which causes i_{RF} to flow.

Figure 8 shows a plot of rectification efficiency measured at 220 MHz for a 1N914 diode, which exhibits a rectification behavior typical for semiconductor junctions. At low RF power levels, the rectification efficiency is independent of the RF power level, and depends only on the bias voltage (and frequency). This is the small signal (square law) region. At higher power levels, approximately 0.2 mW in Figure 8, the rectification efficiency becomes highly dependent on the RF power level and rectification becomes a large signal phenomenon. In this region, the rectification efficiencies for different bias voltages approach each other asymptotically and become proportional to $(P_{RF})^{-1/2}$ which is the proportionality used in large signal models of diodes and transistors[1].

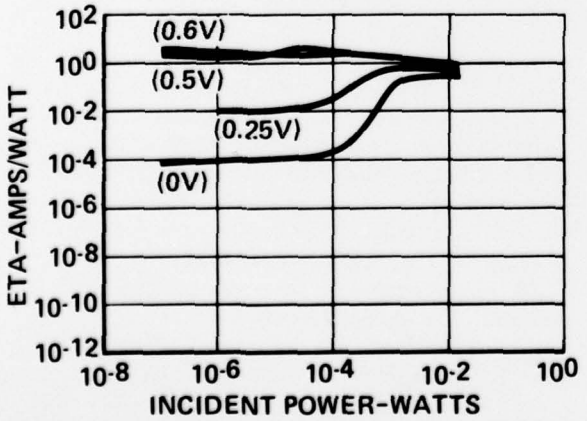


Figure 8. Measured Rectification Efficiency for 1N914 Diode at 220 MHz Versus Bias Voltage and RF Power Level

4.2 Rectification Theory Using Fourier Analysis — Rectification in PN junctions can be studied using a Fourier expansion method. This approach is much more convenient than a time domain approach, and is applicable over a wider range of RF power levels than a small signal approach. In the Fourier analysis, the levels of the higher harmonic voltages and currents are assumed small in relation to the fundamental voltages and currents. This is true for sufficiently small RF power levels.

Figure 9 illustrates the rectification efficiency

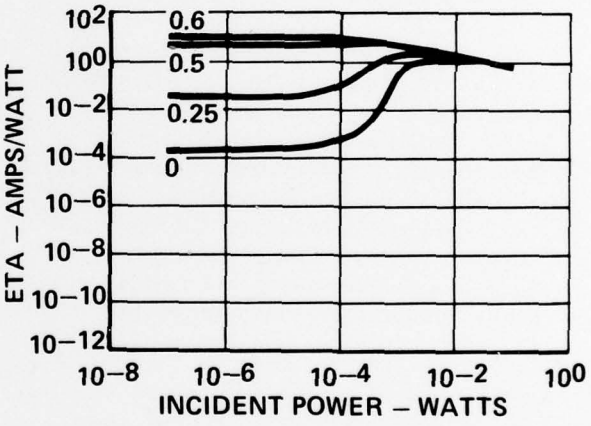


Figure 9. Calculated Rectification Efficiency for 1N914 Diode at 220 MHz Versus Bias Voltage and RF Power Level

predicted for a 1N914 diode at 220 MHz using the Fourier method and diode parameters measured in the laboratory. Comparison with Figure 8 shows the method capable of predicting the large variations in rectification efficiency which occur with bias voltage and RF power variations.

4.3 Worst Case Analysis of Junction Rectification — A simple circuit model for rectification in a PN junction is shown in Figure 10. Diode D1 models the diode junction in the absence of RF energy,

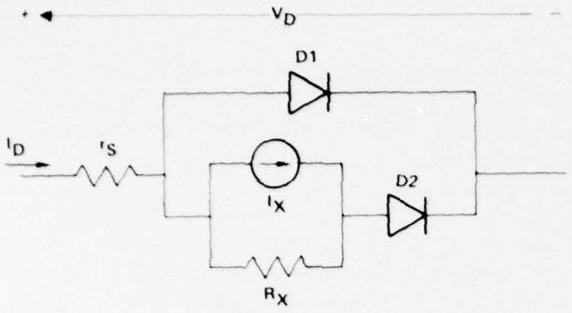


Figure 10. Diode Rectification Model

and can be represented either as ideal or with an exponential current-voltage characteristic. Elements D2, I_X and R_X model the current and voltage offsets which occur when RF stimulus is applied to the junction. Diode D2 is assumed similar in characteristics to diode D1. I_X and R_X depend on the RF frequency, power level, and the RF source impedance. Resistor r_S includes the lossy elements associated with the diode and external circuit.

In the analysis of interference effects in circuits, the RF source impedance is usually unknown, or is very difficult to determine. Since the RF source impedance affects the values of the elements in the rectification model, it is desirable to determine the effect on the circuit for all possible values of source impedance, and design for the worst possible effect. Figure 11 shows the range of the model parameters (normalized, in this case) considering all values of RF source impedance. The

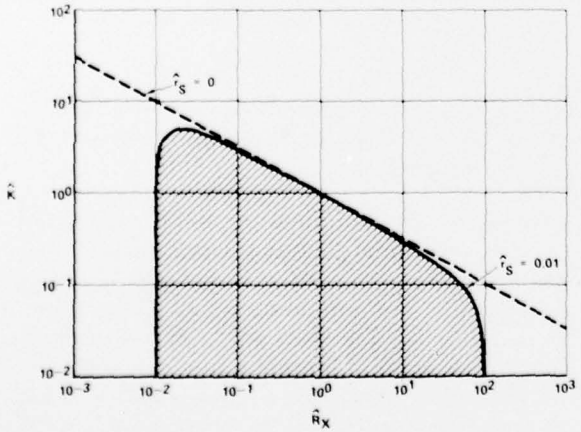


Figure 11. Expected Range of K and R_X

value of I_X is related to the RF power level by

$$I_X = KP_{RF}^{1/2}, \quad (2)$$

where K is a factor which depends on the RF frequency and source impedance. In Figure 11, the possible values of R_X and K lie within the shaded region for a diode with loss (a nonzero value of r_S). The value of R_X is located within a finite interval, and for each value of R_X there exists a maximum value of proportionality factor K. With a lossless diode, however, R_X can assume any positive real value. In this case, all points below the dashed line in Figure 11 are possible values of K versus R_X. The equation for the maximum value of K versus R_X (the dashed line in Figure 11) is[2]

$$K_{max} = (8/R_X)^{1/2}. \quad (3)$$

The range of values for the lossless diode includes all values in the lossy case, so a lossless diode is clearly a worst case assumption.

In the worst case analysis of a circuit, the values of R_X and K for the rectification models are chosen from Figure 11, and the circuit response is calculated for each set of values. By choosing different values of R_X and K through an iterative procedure, the worst case interference response can be found.

4.4 Simulation of Interference in TTL NAND Gates — The circuit analysis program SPICE (Simulation Program with Integrated Circuit Emphasis) was used to simulate interference effects in a 7400 NAND gate. SPICE was developed specifically for analyzing integrated circuits under normal conditions when no interfering signals are present. It is commonly used by circuit designers, integrated circuit manufacturers, and universities. Reference [3] describes the program, its availability, and its input code.

Earlier investigations[4] showed the 7400 NAND gate most susceptible to RF conducted into its output terminal when the output voltage is low (<0.4V), which occurs when both input voltages are high (>2.0V). RF signals conducted into the output terminal can cause the output voltage to change from a normal low state to an RF-induced high state. This is the situation that was simulated with SPICE. The interference was assumed to occur in the NAND gate output transistor, which was modeled in the simulations with a modified Ebers-Moll transistor model[5]. The output transistor was assumed similar to a 2N2369A transistor in characteristics, and the modified Ebers-Moll transistor parameters used were measured in the laboratory for the 2N2369A at 220 MHz.

Three types of TTL NAND gates were investigated to determine their relative susceptibilities to RF interference. These were the normal 7400 series, the high speed 74H00 series, and the low power 74L00 series. The three NAND gate series use different values of internal resistance, which are easily changed in the SPICE simulations. The effect of different fanout values was also investigated by varying the values of load resistors external to the NAND gate in the simulations.

Figure 12 shows a plot of the predicted values of the NAND gate output voltage VOUT versus the incident RF power PINC, which are in good agreement with experimentally measured values[2].

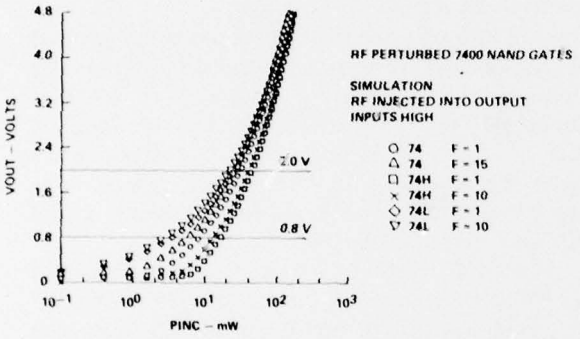


Figure 12. Output Voltage vs. Incident RF Power From SPICE Simulations of Three 7400 NAND Gate Types with Different Fanouts. Susceptibility Thresholds at V_{OUT} Equals 0.8 and 2.0 Volts are Shown.

The plots show the relative susceptibilities of the three NAND gate types with low fanouts (F = 1) and with high fanouts (F = 10 or 15). When no RF power is applied, the output voltage is low (approximately 0.1V). As the RF power increases, the VOUT values increase until they cross the two susceptibility threshold levels. The threshold at VOUT = 0.8V corresponds to the highest voltage that a subsequent stage is guaranteed to recognize as a low state input. The value VOUT = 2.0V corresponds to a VOUT certain to be recognized as a high state (instead of a low state) by a subsequent TTL input. The values of RF power which cause these two threshold levels to be exceeded are easily determined from Figure 12 for each NAND gate type.

The results shown in Figure 12 indicate that the low power 74L00 series NAND gate is the most susceptible to RF interference, while the high speed 74H00 series is the least susceptible. For each NAND gate type the fanout value has a small effect (less than 2 dB difference between minimum and maximum fanout) upon the RF power required to cause the threshold levels to be exceeded.

4.5 Worst Case Analysis of 7400 NAND Gate — When a NAND gate is located in an arbitrary electromagnetic environment where RF signals may be picked up by wires and cables, the possible characteristics of the equivalent RF source seen by the IC may vary widely. An induced RF signal can be represented by a Thevenin equivalent containing a voltage source and a series impedance, which is usually unknown. A worst case analysis of a 7400 (standard series) NAND gate was performed where the value of the RF source impedance was assumed completely arbitrary.

As in the preceding section, the RF signal was conducted into the output terminal of the 7400 NAND gate. Both inputs were assigned a high state voltage, which means the output voltage is a low state in the absence of RF. The RF was assumed to affect only the collector-base junction of the output transistor, which had been shown in earlier simulations to give the worst case results. The collector-base junction rectification parameters were assigned using the worst case information described briefly in Section 4.3, and the collector-base junction was assumed lossless.

The program SPICE was used to perform the worst case analysis of the 7400 NAND gate. The fanout was set to 15, since results of the previous section indicate that high fanouts lead to EM susceptibility at slightly lower RF power levels than low fanouts. Values of RGC (R_X in the collector-base junction of the output transistor) were chosen between 5 and 5000 ohms, and ISCC (I_X in the collector-base junction of the output transistor) was calculated from Equations (2) and (3).

Figure 13 shows values of VOUT versus PINC from the SPICE simulation results. Ten different values of RGC, and the corresponding values of ISCC, were simulated. It can be seen that the value of RGC is quite influential in determining the shape of the VOUT versus PINC curve, and in determining the RF power levels at which various susceptibility threshold levels are crossed. From Figure 13, the values of incident power required to cause the output voltage to cross threshold levels of 0.4, 0.8 and 2.0 volts were determined for each simulation. These values are shown plotted in Figure 14 versus the value of RGC for that case.

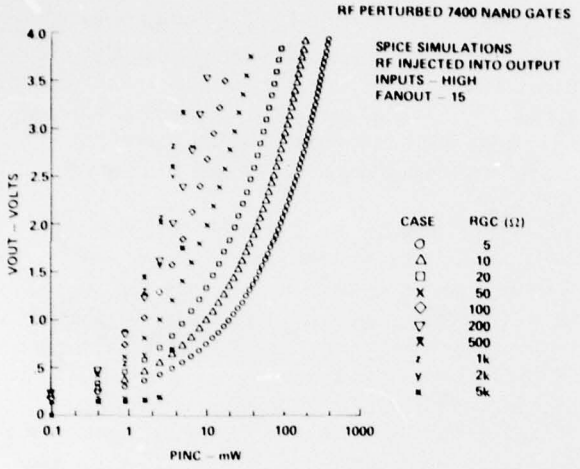


Figure 13. SPICE Simulation Values of Output Voltage Versus Incident RF Power Level for a 7400 NAND Gate

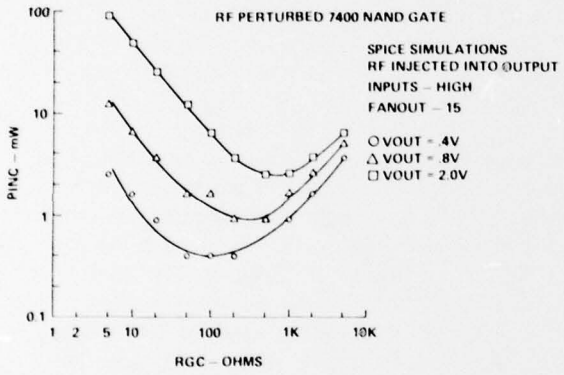


Figure 14. Values of Incident RF Power Required to Cause Output Voltage of 7400 NAND Gate to Exceed Susceptibility Threshold Levels Versus the RF Thevenin Source Impedance

Three curves are shown (one for each threshold level). For each susceptibility threshold in Figure 14 the PINC versus RGC plot has a minimum PINC value. The minimum values of PINC for each threshold are the worst case estimates of the minimum incident RF power to cause the susceptibility threshold levels to be exceeded. These worst case power levels compare favorably with worst case results measured in the laboratory for TTL devices.

4.6 Simulation of Interference in 741 Op Amps — The 741 op amp has been studied for the case of RF entering the input, which is the most susceptible terminal. The study utilized macromodeling techniques, and a full-scale simulation of the complete circuit was done for comparison of the results. The modified Ebers-Moll transistor model was used to account for the interference effect, which was assumed to occur only in a single input transistor.

The op amp macromodel used was developed by Boyle, et. al.[6], and is illustrated in Figure 15. Much of the internal structure of the op amp has been replaced with functional equivalents. This reduces the computer time required to obtain a solution, because the macromodel has fewer elements than the operational amplifier, and because much of the circuit consists of linear elements. Terminally, however, the op amp macromodel behaves as an actual op amp.

A significant feature of the macromodel created by Boyle is that it retains the differential pair configuration at the input terminals, as is found in an actual 741. The two transistors at the input of the macromodel perform the same function as their counterparts in the actual device. The macromodel uses an Ebers-Moll transistor model for each input transistor.

The input transistors were assumed similar to 2N930A transistors in characteristics. With RF entering one of the inputs of the op amp, the interference effect was accounted for by replacing the transistor model at that input with a modified Ebers-Moll transistor model, which includes RF effects. RF parameters were inferred from measured 2N930A interference data at 220 MHz. The effects of beta decreases with increasing power level were included in the model.

The op amp was simulated in a feedback amplifier circuit with a gain of −10. The input voltage was 0.5 volts, so the expected output voltage with no RF was −5.0 volts.

The circuit was simulated on ISPICE, a time-sharing version of the program SPICE which is available through National CSS, Inc. Information on ISPICE features and command structure can be found in Reference [7].

Curve (a) in Figure 16 shows the output voltage of the circuit vs. RF power level when RF enters the inverting input and compares it to data measured in the laboratory[8]. Curves (b) and (c) are the results of two other simulations of the same circuit. To obtain Curve (b), a complete model of the 741 op amp was simulated. The simulations used the computer program SPICE2, an updated version of SPICE. Figure 17 shows a schematic

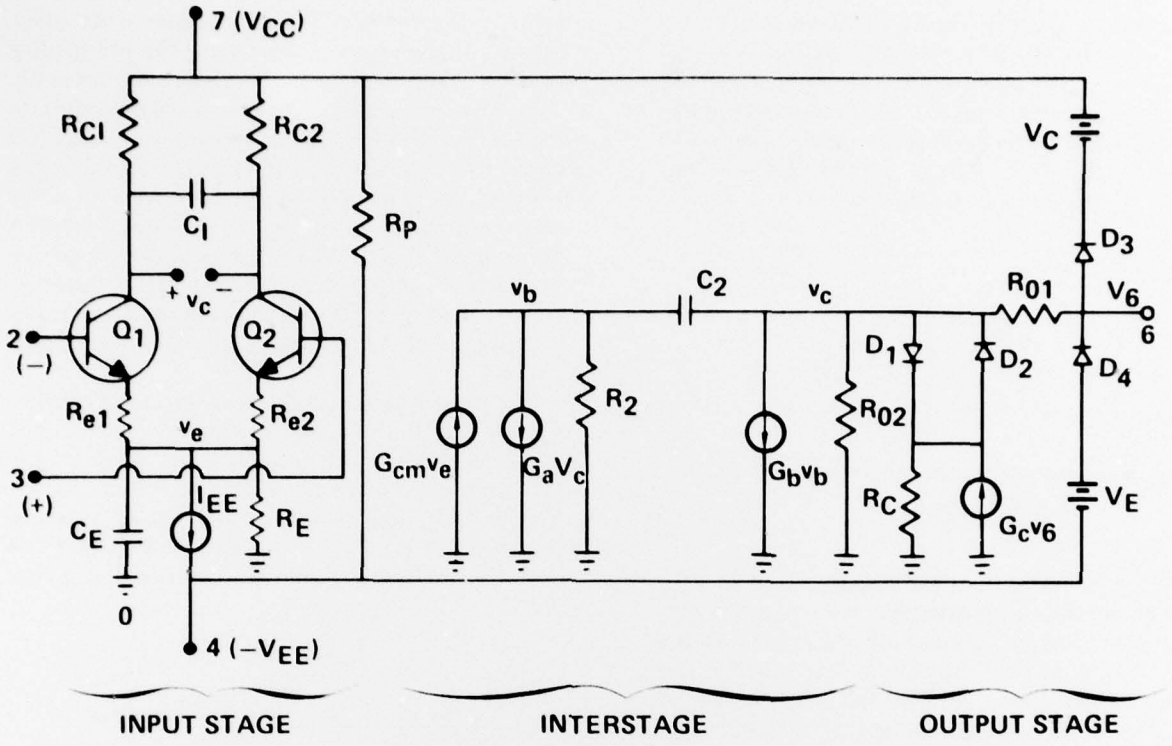


Figure 15. 741 Op Amp Macromodel

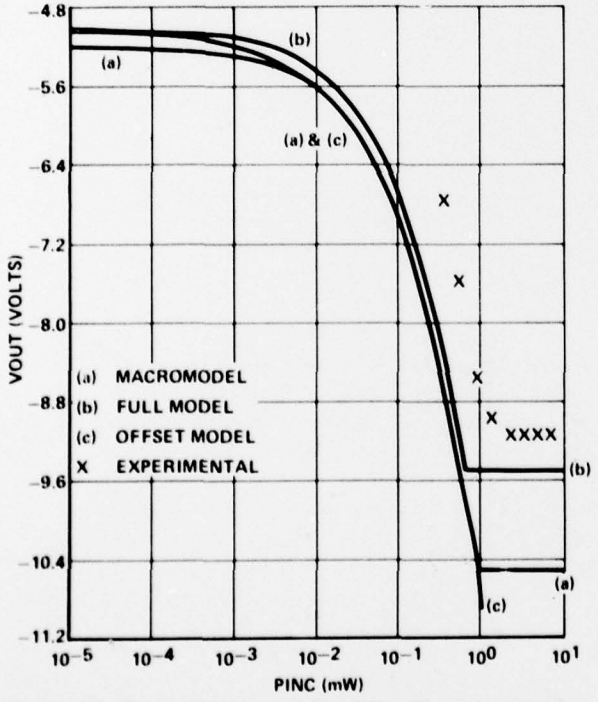


Figure 16. Output Voltage of Amplifier Circuit vs. Incident RF Power. RF Conducted into Inverting Input of 741 at 220 MHz.

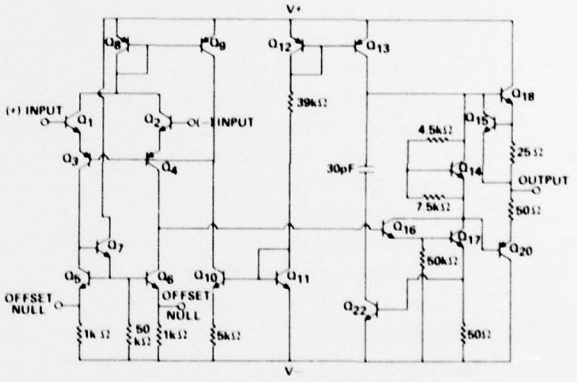


Figure 17. Schematic Diagram of 741 Op Amp Used in Complete Circuit Simulations

diagram for a 741 op amp. Both of the input transistors were modeled using the modified Ebers-Moll transistor model (the RF power entering the transistor at the noninverting input was assumed zero, however). Standard SPICE2 components were used for all other op amp components.

Curve (c) was obtained with a simplified offset model of interference in the op amp. The interference effect was modeled with an offset voltage generator located at the op amp inverting input

terminal as shown in Figure 18. Good correlation has been found between the output voltage predicted by the offset model, and that predicted by the computer calculated simulations where the offset voltage generator has the same value as the RF-induced offset voltage in the base-emitter junction of the input transistor.

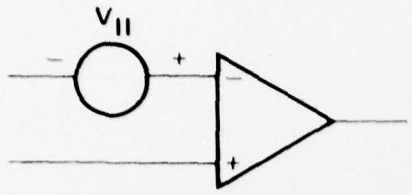


Figure 18. Op Amp Interference Model with Input Offset Generator

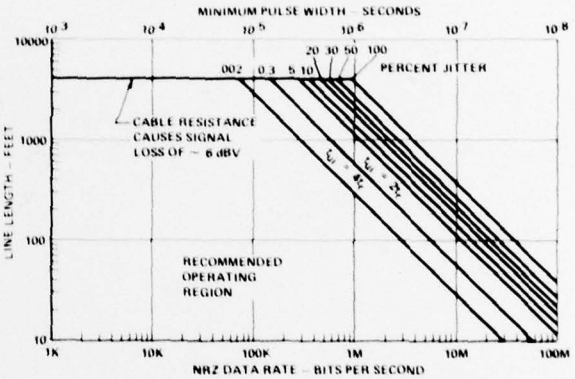
Figure 16 shows that the results obtained with each of the three simulations are comparable. The complete model is fairly accurate in predicting the saturation voltage of the op amp. The macromodel saturates approximately 1.4 volts below the actual circuit. Closer agreement can be obtained by adjusting the macromodel parameters to obtain the desired saturation voltage (in the macromodel, the saturation voltage is independent of the RF effects). The offset model does not saturate, because it assumed an ideal op amp.

The offset voltage which occurred at low RF powers in the macromodel simulation could have been avoided if both input transistors were modeled with modified Ebers-Moll models, as in the complete model simulation.

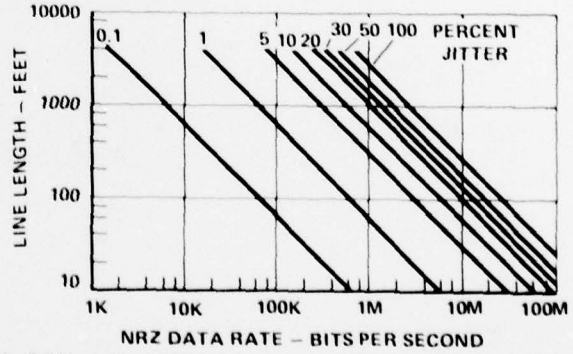
The simulation data is conservative compared to the measured data by about 4 dB. This is reasonable, however, because it was assumed that the incident power affects only the input transistor. In reality, it is unlikely that all of the incident RF power actually reaches the input transistor. Some is probably absorbed in other parts of the chip, or bypasses the input transistor through shunt capacitance.

4.7 Signal Quality in Data Transmission Systems — Investigations into the RF susceptibility of line drivers and receivers have established that the receiver input threshold may change when stimulated by RF. The receiver input threshold is that voltage, applied differentially between the two receiver inputs, at which the receiver output changes state. Threshold offsets, such as those caused by RF, have two undesirable effects on the signal quality in a data transmission system. First, a threshold offset will decrease the noise margin of the system, increasing the probability that bit errors will occur in noisy environments. The second effect, and the one of concern here, is that threshold offsets may cause time variations to occur in the received signal. Comparison of the transmitted and received pulse trains may show that some pulses appear longer or shorter than in the original signal. These time variations can be discussed quantitatively in a term called "percent jitter"[9]. This is a ratio of the maximum variation in pulse position or width to the minimum pulse period.

The jitter was computed analytically, considering the effects of threshold offsets. Figure 19(a) shows the percent jitter as a function of line length and data rate when no threshold offsets occur. Figure 19(b) shows the percent jitter when a threshold offset of $\pm 0.2\ V_{cc}$ is possible, where the line is assumed to be driven by voltages of $\pm V_{cc}$.



a) $V_{th} = 0$



b) $-0.2\ V_{cc} \leq V_{th} \leq 0.2\ V_{cc}$

Figure 19. Signal Quality as a Function of Line Length *and Data Rate Including Effects of Threshold* Voltage Offsets

These graphs were made using parameters for a typical twisted pair line. Reference [9] recommends that systems be operated with jitters less than 0.01% for reliable operation. Data with jitters greater than 100% are probably not recoverable.

Information on threshold offsets in line receivers versus RF power level has been measured experimentally. Figure 4 shows worst case susceptibilities of line receivers in terms of threshold voltage offsets. (For the drivers and receivers that were tested, the line is driven by ±5 volts). Figure 4 can be used in conjunction with Figure 19 to estimate the signal quality in terms of RF power and frequency. The important point for circuit and system designers is that when line driver and receiver systems are required to operate in harsh electromagnetic environments, data transmission rates may have to be slowed in order to ensure reliable data communications.

5. ELECTROMAGNETIC SUSCEPTIBILITY SEMINARS

Three Electromagnetic Susceptibility Seminars have been held during Phase III of the contract, the last two of which were held during this increment. The second Electromagnetic Susceptibility Seminar was held 19-20 October 1977 and had 83 attendees, while the third was held 25-26 October 1978 and had 46 attendees. All three seminars were held at the McDonnell Douglas Headquarters Building in St. Louis, and were jointly sponsored by the Naval Surface Weapons Center/Dahlgren Laboratory and McDonnell Douglas Astronautics Company-St. Louis.

Although the first seminar was concerned mainly with integrated circuit susceptibility, the later seminars also included information on coupling and shielding, hardening design, system susceptibility and testing (including shielding effectiveness testing, laboratory EMV testing and full scale testing).

Included in the first two seminars were discussion sessions where valuable feedback was obtained on the Integrated Circuit Electromagnetic Susceptibility Handbook. Discussions centered around such topics as coupling approaches, shielding within electronic systems, RF impedances of integrated circuits, the RF susceptibilities of devices and technologies that were not specifically covered in the handbook, including microprocessors, low-power Schottky TTL devices, NMOS, etc., and the evaluation of interference when more than one interference source is present. Wherever possible, the comments that were received in these discussions were incorporated into the final version of the IC Handbook.

At the final seminar a special session was devoted to use of the IC Handbook, and included specific examples of determination of pickup levels, susceptibility levels for specific equipment, and shielding levels required to make the equipment satisfy customer specifications.

Based on our experience with these seminars, it appears that the ICES Handbook has been well received by the EMC community and is currently being used for a number of EMC related activities. Comments on the handbook have, in general, been favorable, and most users that have been in contact with MDAC consider it a valuable reference.

6. CONCLUSIONS AND RECOMMENDATIONS

This report is the final output of the Integrated Circuit Electromagnetic Susceptibility Investigation conducted by MDAC. The program has been successful in characterizing, through both measurements and analytical approaches, the electromagnetic susceptibility properties of integrated circuits. The major output of this investigation was the ICES Handbook, which was published 1 August 1978. It summarizes the susceptibility information gleaned during this investigation in a form which can be readily applied to a variety of EMC design and analysis activities.

While integrated circuit technology may change rapidly in the coming years, and increasingly complex circuits may appear, the basic information contained in the ICES Handbook is expected to remain an accurate estimate of the susceptibilities of future integrated circuits. The reason for this is that the present interference mechanism, rectification, is not expected to change with advances in circuit complexity or technology. The handbook is expected to remain a valuable reference for many years to come. Based on verbal feedback and on the seminar attendance, the ICES Handbook has been favorably received, and is currently being used by the EMC community.

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This report summarizes progress made in investigations into the RF susceptibility of integrated circuits (ICs). This report covers the work performed during the third of three increments. Includes is a description of the revisions which were incorporated into the Integrated Circuit Electromagnetic Susceptibility Handbook (Report MDC E1929 dated 1 August 1978) which summarized all of the information obtained during the entire program in a handbook format for use by designers and EMC engineers. Results of tests of

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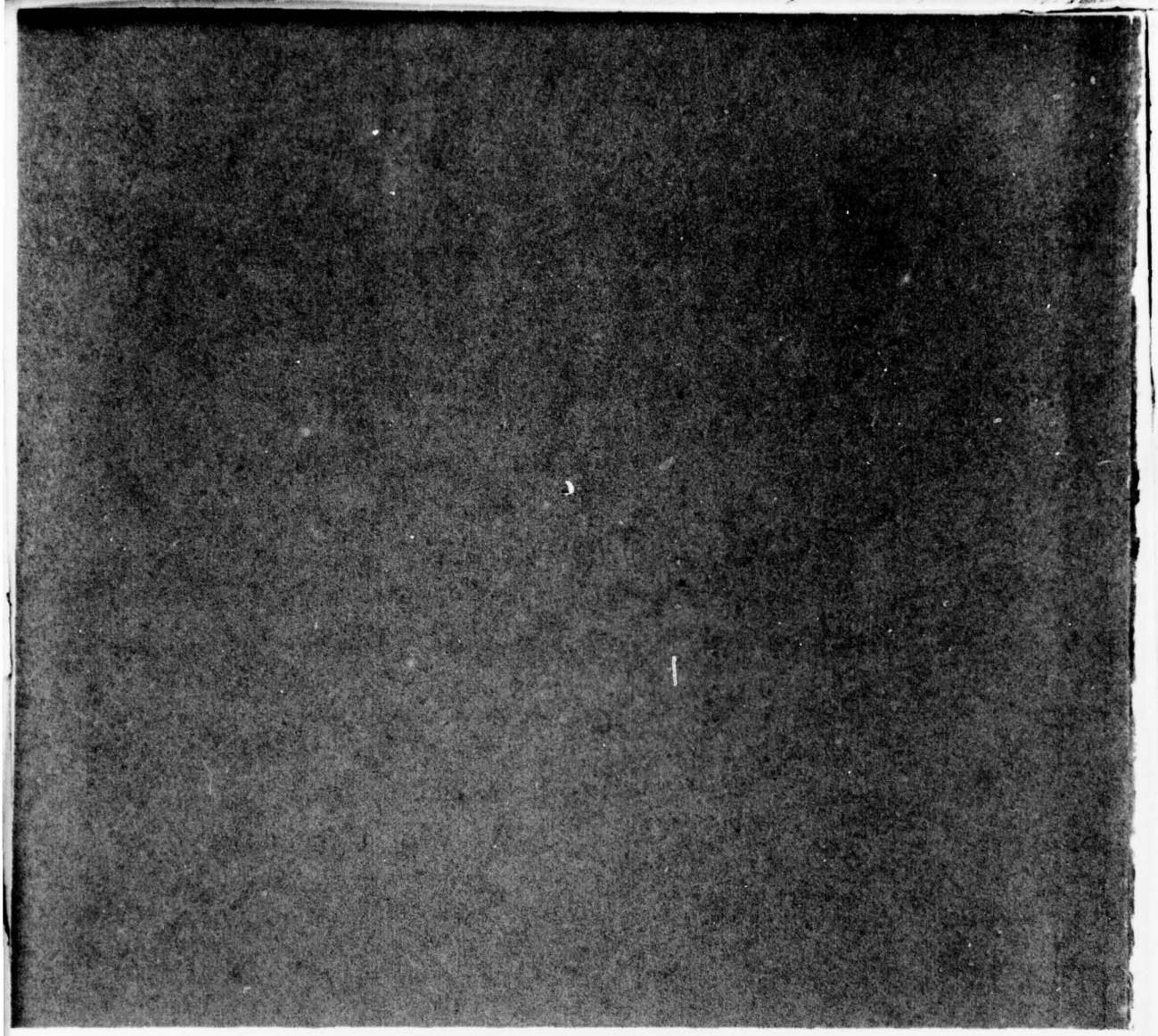
the susceptibilities of integrated circuits performed during this increment are described. Models of rectification in PN junctions developed during this increment are described. Simulations of interference effects in TTL NAND gates and 741 OP AMPs are included using computer-aided circuit analysis techniques and a modified Ebers-Moll transistor model which includes interference effects. Jitter effects due to RF interference in data transmission systems are discussed. This report includes a brief description of two Electromagnetic Susceptibility Seminars which were held during this increment.



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